NCR

DEVICE OPERATION

Data is stored in SNOS memory transistors by applying positive writing pulses that selectively tunnel charge into the nitride at the gate of the transistor. When the writing voltage is removed, the charge trapped in the nitride results in a positive shift in the threshold of the selected SNOS transistor. A negative bias across SNOS transistors reverses this process resulting in a negative shift in threshold for data erasure.

The memory stores sixteen words of sixteen bits each. All functions except the block erase are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

READ CYCLE

Read-out is done in three steps. First, the 4-bit serial address is shifted in on the I/O Pin and into the address register while the Serial Address In code is applied to the three control pins. Next, the Read instruction is strobed in using one clock pulse. This will read the word from the location in the address register and place it into the data register. Finally, while applying the Serial Data Out code, data is shifted out with 16 clock pulses.

WRITE CYCLE

To write new data in, first the address must be changed if the location is different than that in the address register. Then, while applying the Serial Data In code, data is shifted into the data register with 16 clock cycles (unless data to be written is already in the register). Next, the Word Erase code is applied and, after erase time t_E min., the Write code is applied and held for at least t_W min.

When a Read mode immediately follows a Word Erase or Write mode (for the same memory location), one of two options must be used in order to ensure a valid Read operation:

Option 1: Maintain a Read mode (CTR3 = 0, CTR2 = 1, CTR1 = 1) for at least two clock cycles before implementing the Serial Data Out mode (1,1,0).

Option 2: Place the device in a Standby mode (0,0,0 or 1,1,1) for at least one clock cycle before implementing the Read mode (0,1,1).

BLOCK ERASE

The entire memory is erased when BE is held high for t_E min. To ensure a proper Block Erase, the clock should he held low for the entire erase cycle, and the mode of operation prior to the Block Erase should be either Standby (0,0,0 or 1,1,1), Read (0,1,1), Serial Data In (1,0,1) or Serial Address In (0,0,1). A t_{WAIT} time (defined as the negative edge of BE to the positive edge of the clock) of 8 μs must be observed if a Read mode is to immediately follow a Block Erase.

STANDBY

Both Standby codes produce the same results. The memory is placed in an inactive state, the I/O is in a high-impedance state and the clock will have no effect on the device.

PIN DESCRIPTION

CLK - The clock signal is active high, and used for shifting addresses and data into their respective registers and latching control signals.

I/O - The I/O pin is used for inputting data and addresses, and outputting data.

$\overline{CE}$ - Chip enable is active low, and when high will block the clock signal and put the I/O pin into a high-impedance state. It should be noted that when $\overline{CE}$ is high, the device is not automatically placed into a standby mode.

BE - Block erase is active high and used to clear the entire memory. To accomplish block erase, the BE Pin must be held high for t_E. This pin can be tied to V_{SS} during normal operation.

MEMORY MARGINING

The NCR 52801 supports margining of the memory transistors. Memory margining allows device retention time to be projected for the purpose of device evaluation. An application note describing the memory margining algorithm is available.

COMMENTS

- The device should not be in the programming mode (i.e. Erase or Write) during power-up or power-down.
- Erased state results in logical zero at I/O during data output.
- In order to protect data during power-up or power-down, one of the following conditions must exist:
  - — CS held high — Control Lines held low
  - — CLK held low — Control Lines held high

MODE SELECTION

Mode	CTR3	CTR2	CTR1
Standby	1	1	1
Word Erase	1	0	0
Write	0	1	0
Serial Data Out	1	1	0
Serial Address In	0	0	1
Serial Data In	1	0	1
Read	0	1	1
Standby	0	0	0

ABSOLUTE MAXIMUM RATINGS

Voltage on Any Pin
Relative to V_{SS} . . . . . +8 to −0.5V
Storage Temperature (Without
Data Retention) . . . . . −65 to +150°C

Stress above "absolute maximum ratings" may result in damage to the device. Functional operation of devices at the "absolute maximum ratings" or above the recommended operational limits stipulated elsewhere in this specification is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	52801 Min	52801 Typ.	52801 Max.	52801I Min.	52801I Typ.	52801I Max.	Units
V_{CC}	Supply Voltage. (See NOTE 1)	4.5	5.0	5.5	4.5	5.0	5.5	V
V_{IH}	Input High Voltage	2.0		V_{CC} + 1	2.0		V_{CC} + 1	V
V_{IL}	Input Low Voltage	−0.1		0.8	−0.1		0.8	V
T_A	Ambient Temperature	0		70	−40		85	°C

NOTE 1. V_{CC} must be applied at least 100μs before proper operation is achieved.

STATIC ELECTRICAL CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Condition	52801 Min	52801 Typ.	52801 Max.	52801I Min.	52801I Typ.	52801I Max.	Units
I_{IN}	Input Current	V_{in} = 0 TO V_{CC}			10			10	μA
I_{CC}	V_{CC} Supply Current	V_{CC} = 5.5V			15			20	mA
V_{OL}	Output Low Voltage	I_{OL} = 1.6 mA			0.4			0.4	V
V_{OH}	Output High Voltage	I_{OH} = −0.1 mA	2.4			2.4			V
T_S	Non-Volatile Data Storage Time	Following Min. Erase and Write Timings, $N_{EW} \leq 10^4$ Cycles	10			10			Yr.

AC CHARACTERISTICS OVER RECOMMENDED OPERATING CONDITIONS

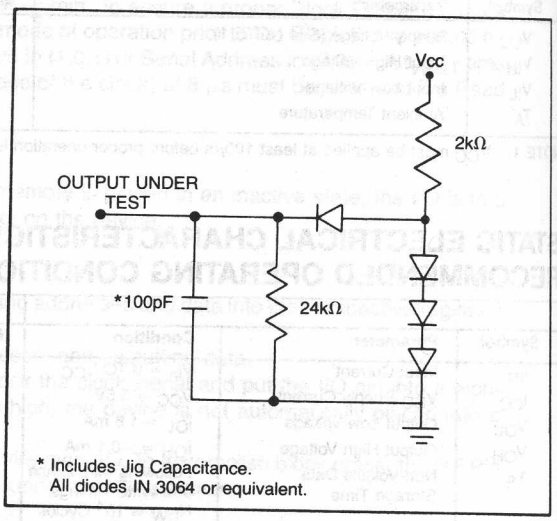
Symbol	Parameter	Min.	Typ.	Max.	Unit
t_E	Erase Time	100			ms
t_W	Write Time	10		50	ms
t_{CHCL}	Clock High Level Hold Time	4		10	µs
t_{CLCH}	Clock Low Level Hold Time	4			µs
t_R	Clock Rise Time	5		1000	ns
t_F	Clock Fall Time	5		1000	ns
t_{SLCH}	Chip Select Setup	1			µs
t_{CLSH}	Chip Select Hold	1			µs
t_{CHQV}	Data Out Delay			1	µs
t_{AVCL}	Address In Setup	1			µs
t_{DVCL}	Data In Setup	1			µs
t_{CLDX}	Data In Hold	200			ns
t_{CTRVCH}	Control Setup	1			µs
t_{CTRX}	Control Hold	50			ns
t_{CHQZ}	Data Off Time From Clock			3	µs
t_{SLQX}	Chip Select Low to Output Active			2	µs
t_{SHQZ}	Chip Select High to Output Inactive			2	µs
$N_{E/W}$	Number of Erase/Write Cycles (See NOTE 2)			10^4	cycles

NOTE 2. The specified maximum of 10^4 cycles will ensure a T_S min. of 10 years, increasing $N_{E/W}$ beyond 10^4 cycles will degrade T_S logarithmically.

A.C. TEST CONDITIONS

Input Timing Levels: 0.8 Volts and 2.0 Volts
Output Timing Levels: 0.8 Volts and 2.0 Volts
Input Rise and Fall Times (except Clock): 20 ns
Input Pulse Levels: 0.45 Volts and 2.4 Volts

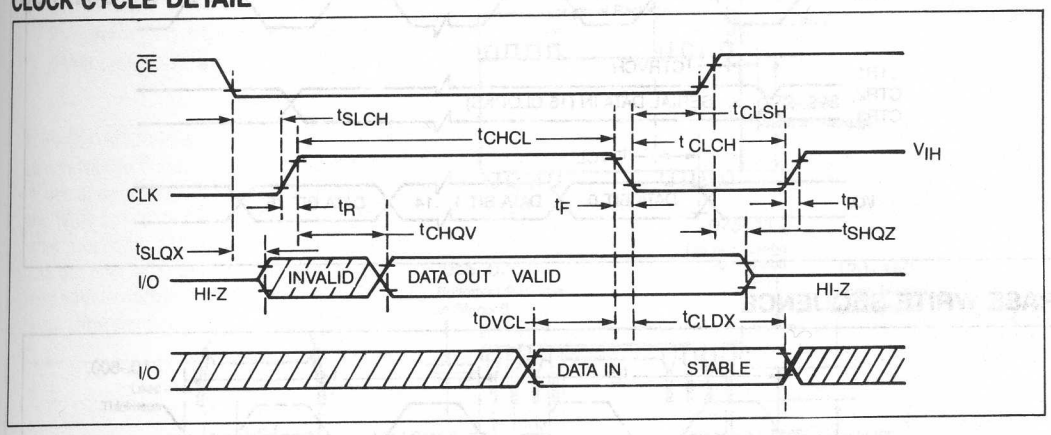
TEST LOAD CIRCUIT



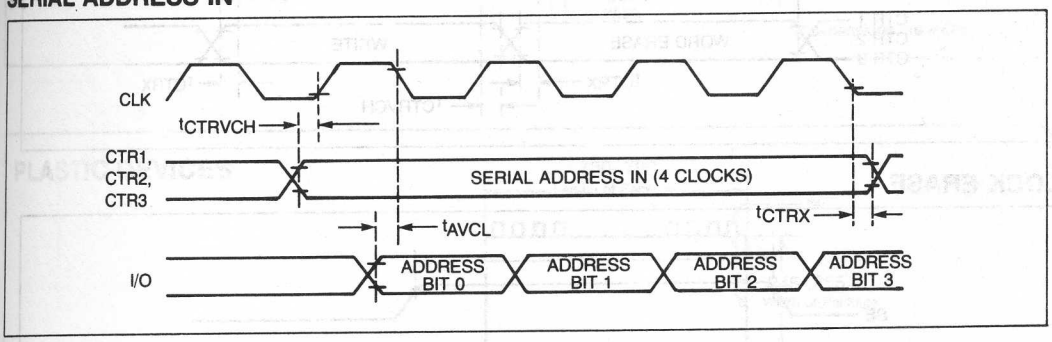
* Includes Jig Capacitance.
All diodes IN 3064 or equivalent.

WAVEFORMS

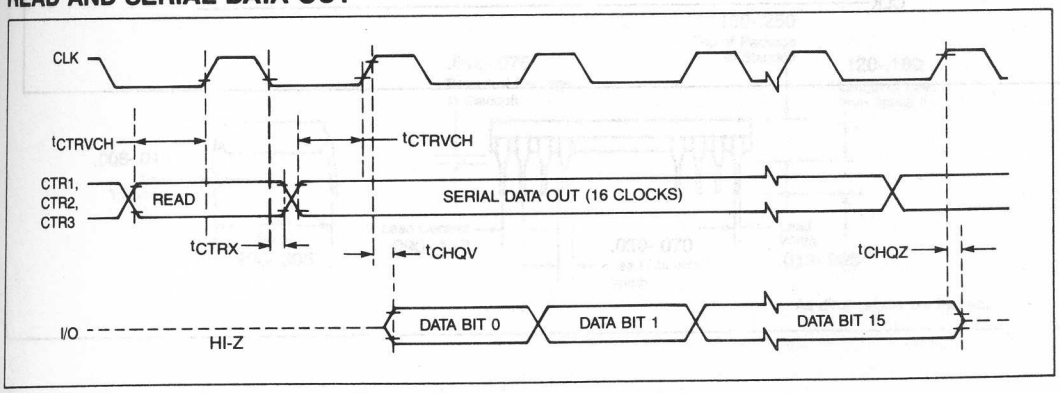
CLOCK CYCLE DETAIL



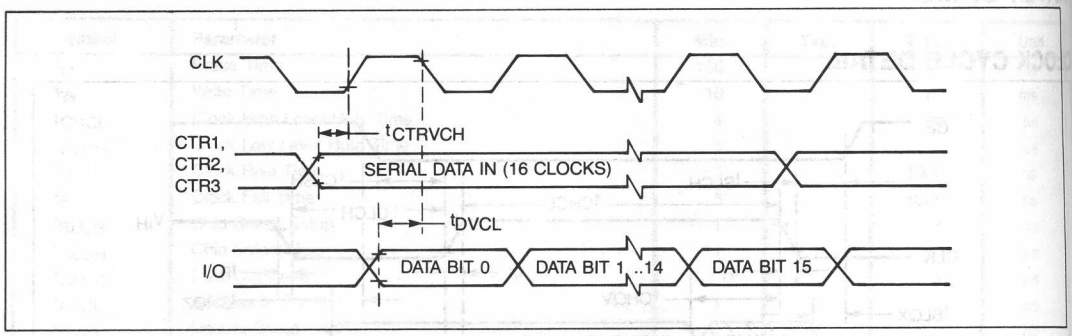
SERIAL ADDRESS IN



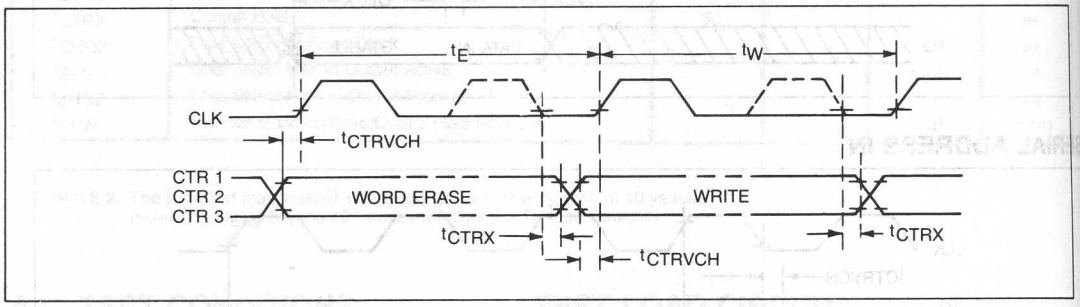
READ AND SERIAL DATA OUT



SERIAL DATA IN



ERASE WRITE SEQUENCE



BLOCK ERASE