NCR

DEVICE OPERATION

Data is stored in SNOS memory transistors by applying positive writing pulses that selectively tunnel charge into the nitride at the gate of the transistor. When the writing voltage is removed, the charge trapped in the nitride results in a positive shift in the threshold of the selected SNOS transistor. A negative bias across SNOS transistors reverses this process resulting in a negative shift in threshold for data erasure.

The memory stores sixteen words of sixteen bits each. All functions except the block erase are selected by a 3-bit parallel control code. The clock line is used to strobe these codes and to serially shift data and addresses.

READ CYCLE

Read-out is done in three steps. First, the 4-bit serial address is shifted in on the I/O Pin and into the address register while the Serial Address In code is applied to the three control pins. Next, the Read instruction is strobed in using one clock pulse. This will read the word from the location in the address register and place it into the data register. Finally, while applying the Serial Data Out code, data is shifted out with 16 clock pulses.

WRITE CYCLE

To write new data in, first the address must be changed if the location is different than that in the address register. Then, while applying the Serial Data In code, data is shifted into the data register with 16 clock cycles (unless data to be written is already in the register). Next, the Word Erase code is applied and, after erase time t_E min., the Write code is applied and held for at least t_W min.

When a Read mode immediately follows a Word Erase or Write mode (for the same memory location), one of two options must be used in order to ensure a valid Read operation:

Option 1: Maintain a Read mode (CTR3 = 0, CTR2 = 1, CTR1 = 1) for at least two clock cycles before implementing the Serial Data Out mode (1,1,0).

Option 2: Place the device in a Standby mode (0,0,0 or 1,1,1) for at least one clock cycle before implementing the Read mode (0,1,1).

BLOCK ERASE

The entire memory is erased when BE is held high for t_E min. To ensure a proper Block Erase, the clock should he held low for the entire erase cycle, and the mode of operation prior to the Block Erase should be either Standby (0,0,0 or 1,1,1), Read (0,1,1), Serial Data In (1,0,1) or Serial Address In (0,0,1). A t_{WAIT} time (defined as the negative edge of BE to the positive edge of the clock) of 8 μs must be observed if a Read mode is to immediately follow a Block Erase.

STANDBY

Both Standby codes produce the same results. The memory is placed in an inactive state, the I/O is in a high-impedance state and the clock will have no effect on the device.

PIN DESCRIPTION

CLK - The clock signal is active high, and used for shifting addresses and data into their respective registers and latching control signals.

I/O - The I/O pin is used for inputting data and addresses, and outputting data.

$\overline{CE}$ - Chip enable is active low, and when high will block the clock signal and put the I/O pin into a high-impedance state. It should be noted that when $\overline{CE}$ is high, the device is not automatically placed into a standby mode.

BE - Block erase is active high and used to clear the entire memory. To accomplish block erase, the BE Pin must be held high for t_E. This pin can be tied to V_{SS} during normal operation.